Electronically filed October 23, 2012

IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

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| Application of: | Sudhakar Muddu | Confirmation No.: | 4796 |
| Serial No.: | 09/713,842 | Art Unit | 2125 |
| Filed: | November 15, 2000 | Examiner: | Paladini, Albert Williams |
| For: | Method and System for Estimating Interconnect Delay | Attorney Docket No.: | 001361-5140-US |

STATEMENT UNDER 37 C.F.R. § 3.73(b)

Commissioner for Patents
P.O. Box 1450
Alexandria, VA 22313-1450

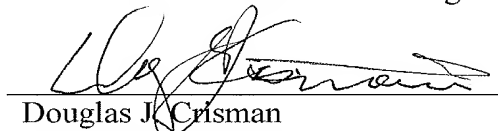
Sir:

Silicon Graphics International Corp., a corporation, states that it is the assignee of the entire right, title and interest in the parent of the patent application identified above by virtue of an assignment from the inventor(s) in the parent of the patent application/patent identified above:

| | | | | | | |
|---|---|---|---|---|---|---|
| 1. | From: | Sudhakar Muddu | | | | |
| | To: | Silicon Graphics, Inc. | | | | |
| | Recorded: | April 16, 2002 | Reel: | 012818 | Frame: | 0542 |
| 2. | From: | Silicon Graphics, Inc. | | | | |
| | To: | Silicon Graphics International Corp. | | | | |
| | Recorded: | February 16, 2012 | Reel: | 027727 | Frame: | 0020 |

The undersigned is authorized to act on behalf of the assignee.

Date: October 23, 2012



39,951
(Reg. No.)

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